RZ RECOVERY

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims benefit of U.S. Provisional Application No. 60/266,395 filed on February 1, 2001 which is hereby incorporated by reference as if set forth in full herein.

BACKGROUND OF THE INVENTION

The present invention relates generally to clock recovery circuits and methods and in particular to systems and methods performing clock recovery for return-to-zero (RZ) serial data stream.

Modern communication systems transfer tremendous amounts of data at ever increasing rates. Various transmission schemes and encoding of data are utilized to assist in the transfer. One particular type of encoding scheme for digital data transmission is a return-to-zero (RZ) data stream. A RZ data stream transmits digital data in which a logical one and a logical zero are determined based on voltage pulses having certain or specific characteristics. In particular, a logical one or zero is determined by the voltage during a first half of each bit. The signal returns to a resting state, typically zero volts, during the subsequent or remaining half of the bit. Additionally, there are two types of RZ data, a positive logic RZ data and negative logic RZ data.

In positive-logic RZ data, a logical zero is represented by a voltage that is more negative or less positive then the voltage that represents a logical one. Conversely, in negative-logic RZ data, a logical zero is represented by a voltage that is more positive or less negative then the voltage that represents a logical one.

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Another type of encoding scheme for digital data transmission is a non-return-to-zero (NRZ) data in which a logical one and zero are determined by specific and constant direct-current (DC) voltages. Similar to RZ data, NRZ data has two forms, a positive-logic NRZ data and a negative-logic NRZ data. In positive-logic NRZ data, a logical zero is represented by a voltage that is more negative or less positive then the voltage that represents a logical one. Likewise, in negative-logic NRZ data, the logical zero is represented by a voltage that is more positive or less negative then the voltage that represents a logical one.

Typically, the data stream transmitted in either form, as RZ or NRZ data, is transferred optically and then converted to electrical signals. Subsequently, clock and data information are retrieved from the converted electrical signals. However, optimizing the retrieval of clock and data information from the converted electrical signals is sometimes difficult.

SUMMARY OF THE INVENTION

The present invention provides a return-to-zero recovery system that optimizes data re-timing and improves signal to noise ratio for data recovery.

In one aspect the present invention provides a return-to-zero (RZ) recovery system. The return-to-zero recovery system in one embodiment comprises a filter configured to receive a data signal and to reduce high frequency components from the data signal to form a filtered data signal and a recovery unit configured to receive the filtered data signal identify a first type of data transition and provide phase information when the first type of data transition is identified.

In a further aspect the present invention provides a method

of sampling return-to-zero data. In one embodiment the method comprises receiving a data signal; identifying a transition to a second data state from a first data state; and providing phase information when the transition is identified.

In a further aspect the present invention provides a method of sampling return-to-zero data. In one embodiment the method comprises determining first phase information from a data signal when a first type of data transition occurs; determining second phase information from a data signal when a second type of data transition occurs; generating a first clock signal based on the first phase information; generating a second clock signal based on the second phase information; generating a third clock signal based on the first and second clock signals.

In a further aspect the present invention provides a return-to-zero (RZ) recovery system. In one embodiment the system comprises first recovery unit configured to receive a data signal and identifying a first type of data transition and determining a first phase information when the first type of data transition is identified; and second recovery unit configured to receive the data signal and identifying a second type of data transition and determining second phase information when the second type of data transition is identified.

These and other aspects of the present invention will be more readily understood upon review of the accompanying drawings and following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an embodiment of a receiving unit with a clock and data recovery unit;

FIG. 2 is a block diagram of an embodiment of a clock and data recovery unit;

FIG. 3 is a block diagram of a multiple recovery unit clock signal provider adapted for use with RZ data systems; and

FIG. 4 is a block diagram of a receiver with multiple CRU instantiations.

DETAILED DESCRIPTION

In FIG. 1, a return to zero (RZ) optical pulse waveform is supplied as an input to a receiver 3. The receiver 3 includes a low-pass filter 31 and a non-return to zero (NRZ) clock and a clock and data recovery unit 33. The RZ optical pulse waveform is provided to the low pass filter. The low pass filter removes or attenuates the high frequency components in the RZ waveform. As such, the RZ waveform is largely transformed into a NRZ signal. The NRZ signal is supplied to the clock and data recovery (CDR) unit. The CDR unit extracts the clock signal encoded in the NRZ signal. Hence, a local clock at the receiver is synchronized to the extracted clock signal.

The low-pass filter, by removing or attenuating high frequency components contained in the received RZ waveform performs two functions. The first function is a validation function that detects or qualifies that a one or high level is valid when a specific voltage level is maintained for a specific amount of time. In other words, transient high voltages are filtered out, and do not result in false data readings or otherwise impact system operation. In addition the slope of the rising and falling edges of waveform are somewhat flattened, potentially increasing the size of the data eye. The second function is a phase function that maintains or adjusts the RZ waveform to have a one to zero transition time at approximately the same position with respect to the bit time as a zero to one data transition. A potential problem with the low-pass filter

performing both functions, however, is that sharp transitions in the data-eye are blurred, with negative effects on data-eye shape.

In one embodiment, the CDR unit performs the phase function. Thus, the cut-off frequency of the low-pass filter may be increased, allowing increased frequency components of the signal to improve the shape of the data-eye. The low-pass filter can therefore be optimized to achieve optimal results for the validation function without having to provide a trade off to achieve optimal results to perform the phase function.

In one embodiment, the CDR unit receives RZ waveform as an input. The RZ waveform has zero to one data signal transitions spaced nominally at the start of the bit period. However, one to zero data signal transitions occur at normally less than half the bit period after the zero to one data signal transition. The CDR unit rejects phase information, or alternatively does not perform comparisons to obtain phase information, except at zero to one data signal transitions. As such, the phase detector operates only when data bits prior to and following a perceived zero to one data transition occurs.

FIG. 2 illustrates a block diagram of an embodiment of a CDR unit in accordance with the present invention. In FIG. 2, the CDR unit includes a phase detector 301, an inhibitor 303, a loop filter 305 and a voltage controlled oscillator (VCO) 307. The CDR unit receives a data signal and a reference clock signal, and generates an output clock signal. The phase detector detects the amount by which the phase of the recovered clock signal leads or lags the phase of the transmitted data signal. The phase detector receives the data signal and the output clock signal and generates a phase difference signal. In various embodiments the phase difference signal is based on up/down

signals, increment/decrement signals, or other signals, depending on specific PLL, or DPLL implementations. The phase difference signal is proportional to the difference in phase between the transmitted data signal and the output clock signal. The phase difference signal is provided to the inhibitor.

The inhibitor receives the data signal and determines if a zero to one data transition has occurred. If a zero to one data transition has occurred, the inhibitor provides the phase difference signal to the loop filter. Otherwise, the inhibitor does not provide the phase difference signal to the loop filter. In one embodiment, this is accomplished using shift registers and simple logic, although in other embodiments various circuitry is utilized. In one embodiment, circuitry for performing the inhibitor function is contained within the phase detector block.

The loop filter filters the phase difference signal and provides the filtered phase difference signal to the VCO as a control voltage signal. The VCO generates the output clock signal based on the filtered phase difference signal. The VCO adjusts the oscillation frequency of the output clock signal based on the filtered phase difference signal.

If the phase of the reference clock signal leads the phase of the shifted output clock signal, the filtered phase difference signal indicates a need for a phase shift, i.e., for the shifted variable clock signal to speed up. On the other hand, if the phase of the reference clock signal lags behind the phase of the shifted variable clock signal, the filtered phase difference signal indicates a need for a phase shift, i.e., for the shifted variable clock signal to slow down.

In another embodiment, the inhibitor is placed before the phase detector instead of after the phase detector. The

inhibitor receives the data signal and determines if a zero to one data transition occurs. If a zero to one data transition occurs, the inhibitor provides the data signal to the phase detector. Otherwise, the inhibitor does not provide the data signal to the phase detector. Subsequently, the phase detector provides a phase difference signal to the loop filter. In various embodiments, the CDR unit is composed of analog components and/or digital components.

In FIG. 3, a data signal, e.g., an RZ data signal, is supplied to a first recovery unit 21 and a second recovery unit 23. The first recovery unit extracts a first clock signal from the data signal. Similarly, the second recovery unit extracts a second clock signal from the data signal. The first and second clock signals are provided to an adder or interpolator 25. The interpolator provides an output clock signal based on the first and second clock signals.

In one embodiment, the first recovery unit receives an RZ data signal and recovers a clock signal from the RZ data signal based on rising edge signal transitions. Thus, in some embodiments the first recovery unit rejects phase information, or alternatively does not perform comparisons to obtain phase information, except at zero to one data transitions. As such, for example, a phase detector of the first recovery unit provides for phase adjustment around a perceived zero to one data transition. The first clock signal is therefore adjusted to be in phase with the zero to one transitions in the RZ data signal.

The second recovery unit also receives the RZ data signal and recovers a clock signal from the RZ data based on falling edge signal transitions. Thus, in some embodiments the second recovery unit rejects phase information, or alternatively does

not perform comparisons to obtain phase information, except at one to zero data transitions. As such, for example, a phase detector of the second recovery unit provides for phase adjustment when data bits around a perceived one to zero data transition. The second clock signal is therefore adjusted to be in phase with the one to zero transitions in the RZ data signal.

The interpolator adds the first clock signal and the second clock signal to form an output clock signal. The first clock signal and the second clock signal have rising edges bounding an expected data eye of the RZ data signal. The output clock signal, formed by combining the first clock signal and the second clock signal, has a rising edge, or is in phase with, the expected data eye of the RZ data signal. In some embodiments the combining of the first clock signal and the second clock signal is performed using weighted summers, which also allows for some further phase shift in the output clock signal to more accurately sample in the middle of the data eye.

FIG. 4 illustrates a block diagram of an embodiment of a receiver in accordance with the present invention. In FIG. 4, the receiver receives a data signal. In one embodiment, the data signal is an RZ data signal. The data signal is supplied to two clock recovery units. A first clock recovery unit includes a phase detector 401, a loop filter 403 and a voltage controlled oscillator (VCO) 405. A second clock recovery unit includes a phase detector 501, a loop filter 503 and a VCO 505.

The recovery units generate clock signals that are supplied to an interpolator 61. The interpolator, in one embodiment, compares or adds the clock signals together to generate an output clock signal. The output clock signal is supplied to a sampling unit or an output buffer 45. The output buffer

generates a data signal based on the output clock signal and the incoming data signal.

The phase detector 401 receives the data signal and the clock signal generated by the VCO 405. The phase detector 401 determines if a zero to one data transition has occurred. If a zero to one data transition has occurred, the phase detector determines whether the rising edge of the clock signal is early or late with respect to the data transition and generates a phase difference signal. In one embodiment, if the rising edge of the clock signal is early, a slow, or down, signal is generated. If the rising edge of the clock signal is late a fast, or up, signal is generated. The up/down signals are provided to the loop filter 403. Thus, the phase detector 401 may be viewed in one embodiment as a rising edge phase detector.

In an alternative embodiment, the phase detector determines a phase difference between the data signal and the clock signal. In other words, the phase detector determines the amount by which the phase of the clock signal leads or lags the phase of the data signal, about zero to one transitions in the data signal. The phase detector generates a phase difference signal that, in one embodiment, is proportional to the difference in phase between the data signal and the recovered clock signal. In the alternative embodiment, the phase difference signal is provided to the loop filter.

Returning to FIG. 4, the loop filter filters the up/down signals and provides a filtered up/down signal to the VCO 405. The VCO generates the clock signal based on the up/down signal. As such, the VCO adjusts the oscillation frequency of the output clock signal based on the filtered up/down signal. The clock signal is supplied to the interpolator 61.

The phase detector 501 receives the data signal and the clock signal generated by the VCO 505. The phase detector 501 determines if a one to zero data transition has occurred. If a one to zero data transition has occurred, the phase detector determines whether the rising edge of the clock signal is early or late with respect to the data transition and generates a phase difference signal. In one embodiment, if the rising edge of the clock signal is early, a slow, or down, signal is generated. If the rising edge of the clock signal is late a fast, or up, signal is generated. The up/down signals are provided to the loop filter 503. Thus, the phase detector 501 may be viewed in one embodiment as a falling edge phase detector.

In an alternative embodiment, the phase detector determines a phase difference between the data signal and the clock signal. In other words, the phase detector determines the amount by which the phase of the clock signal leads or lags the phase of the data signal, about zero to one transitions in the data signal. The phase detector generates a phase difference signal that, in one embodiment, is proportional to the difference in phase between the data signal and the recovered clock signal. In the alternative embodiment, the phase difference signal is provided to the loop filter.

Referring back to FIG. 4, the loop filter filters the up/down signals and provides the filtered up/down signal to the VCO 505. The VCO generates the clock signal based on the filtered up/down signal. As such, the VCO adjusts the oscillation frequency of the output clock signal based on the filtered up/down signal. The clock signal is supplied to the interpolator 61.

In one embodiment, a plurality of phase-shifted clock

signals are provided by a single VCO. The frequency of the VCO, for example, is controlled or determined by the rising edge phase detector. The falling edge phase detector outputs are used in forming a selection signal used to select one of the clock signals provided by the VCO.

The interpolator additively mixes the clock signals from the VCOs to form an output clock signal. The output clock signal is provided to the sampling unit. The sampling unit recovers data from the data signal, and, for example, forms an NRZ data signal.

In one embodiment, a filter 43 filters the RZ data signal provided to the sampling unit. The filter filters out the high frequency components of the data signal, and thereby stretches out the data eye of the data signal. Thus, the sampling area of the data eye available to recover the data becomes larger and thereby sampling is easier to perform. In such a variation, the filter 43 also filters, in one embodiment, the RZ data signal provided to the rising edge phase detector and the falling edge phase detector to allow for phase shifts in the data eye due to the filter. In a further embodiment filters 41 and 51 are also available to filter the data signals provided to the clock recovery units. In operation the use of such filters may allow for optimal stretching of the RZ signal to form an NRZ type signal used by the clock recovery units for clock recovery.

Accordingly, the present invention provides for RZ recovery. Although this invention has been described in certain specific embodiments, many additional modifications and variations would be apparent to those skilled in the art. It is therefore to be understood that this invention may be practiced otherwise than as specifically described. Thus, the present embodiments of the invention should be considered in all

respects as illustrative and not restrictive.

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